REMARKS/ARGUMENTS

Applicants have studied the Office Action dated December 23, 2005 and have made amendments to the claims. It is submitted that the application, as amended, is in condition for allowance. By virtue of this amendment, claims 1-3, 6-14, and 16-20 are pending. Claims 1, 7, and 12 are amended. Reconsideration and allowance of the pending claims in view of the above amendments and the following remarks is respectfully requested.

(1-2) Rejection under 35 U.S.C. §102(b) Chen et al.

In the Office Action, the Examiner rejected claims 1-3, 6-14, and 16-20 under 35 U.S.C. § 102(e) as being anticipated by Chen et al. (U.S. Patent No. 6,538,486).

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful. Amended independent claims 1 and 12 recite, *inter alia*:

> ...
> a delay element, the first strobe signal being an input to the delay element; and
> a strobe circuit coupled to the latch circuit, the strobe circuit capturing the output of the latch circuit based on a second strobe signal output from the delay element, wherein the second strobe signal output from the delay element is independent of a phase of the first strobe signal. (emphasis added)

Amended claim 7 recites, *inter alia*:

> ...
> wherein the latch circuit includes:
> an input;
> an input branch and a latch branch connected in parallel between the input and an output; and
> a bias current control transistor coupled in series between the output and both the input branch and the latch branch.

The present invention is a differential data sampling circuit that samples an input signal line with precise timing so as to provide reduced sensitivity to noise. The differential data sampling circuit includes a latch circuit for initially sampling a differential data

signal in response to a first strobe signal. The latch circuit operates to rapidly capture the signal level present on the input signal line. The output of the latch circuit is then sampled by a strobe circuit in order to capture and hold the output of the latch circuit based on a second strobe signal.

The strobe signal that is used to trigger the latch circuit is delayed by a delay element (522) before being supplied to the strobe circuit. The use of a strobe signal that is delayed from the strobe signal input to the latch circuit allows the output of the latch circuit to settle prior to capture by the strobe circuit.

The Chen et al. reference discloses a latch chain with improved input voltage sensitivity. Chen et al. provides a modified latch that is more sensitive to input voltage than a pair of conventional latches that are provided downstream from the modified latch and an amplifier. In Chen et al., all three latches are run from a single output of a clock (22). See, Chen et al., FIG. 2.

The Examiner, on page 3 of the Office Action, states analogizes the delay element (522) of the present invention to the inverter element of Chen et al., shown in FIG. 2. An inverter element, as is known well by those of skill in the art, provides a signal that is 180 degrees out of phase from the input. Inverters, by definition, are expressly dependent on the phase of the input. Therefore, in the Chen et al. circuit shown in FIG. 2, the conventional latch 18 accepts an output signal from the amplifier 16 when the Clk signal is high and the conventional latch 20 accepts an output signal from the convention latch 18 only when the phase of the Clk signal changes by 180 degrees (low).

Importantly, a delay circuit, in contrast to an inverter, is not dependent on a phase of the input. For this reason, the delay element (522) of the present invention can be set at any amount of delay, independent from any phase of an input signal. Because a delay circuit delays a signal by a predefined amount of time, regardless of the phase of its input signal, phase is irrelevant to the delay circuit of the present invention. Therefore, the delay circuit (522) of the present invention is not dependent on a phase

of the strobe signal singal (Strobe (0:n)). The data sampling circuit of the present invention is solely dependent on a preset amount of delay time in the delay circuit (522), which can be any amount of time. Using a delay circuit with a delay not locked to one half of the Clk duty cycle, as is taught by Chen et al., allows use of a shorter delay and allows a shorter propagation time for the entire data sampling circuit to be realized.

Therefore, Chen et al. does not disclose a delay element, *wherein the second strobe signal output from the delay element is independent of a phase of the first strobe signal*, as recited in independent claims 1 and 12 of the instant application.

Continuing further, independent claim 7 has been rewritten in independent form and amended to include the limitations of previously amended claim 1. Amended claim 7, as in its previous form, recites, *inter alia*:

> an input;
> an input branch and a latch branch connected in parallel between the input and an output; and
> a bias current control transistor coupled in series between the output and both the input branch and the latch branch.

On page 4 of the Office Action, the Examiner refers to FIG. 1 of Chen et al. and identifies 2 as the input branch, 5 as the latch branch, A as the input, I_0 as the output, and Clk as the bias current control transistor.

However, a clock circuit (Clk) is not a bias control transistor. Clocks control timing within a circuit, but not the bias of a circuit. In particular, the Clk signal of the prior art circuit shown in FIG. 1 of Chen et al., determines the input branch (2) conducts or not. It does not control bias.

In addition, Chen et al. does not disclose the presence of a transistor in the current source I_0. If the Examiner maintains the contention that the Clk of Chen et al. is analogous to the bias transistor of the present invention, looking at FIG. 1 of Chen et al., it can be seen that Clk is in series with only the input branch (2). Alternatively, the inverse Clk signal is in series with only the latch branch (5). Therefore, Chen et al.

clearly does not show *a bias current control transistor coupled in series between the output and* ***both*** *the input branch and the latch branch.*

The Examiner cites 35 U.S.C. § 102(e) and a proper rejection requires that a single reference teach (i.e., identically describe) each and every element of the rejected claims. Because the elements in independent claims 1, 7, and 12 of the instant application are not taught or disclosed by Chen et al., the apparatus of Chen et al. does not anticipate the present invention. [1] The dependent claims are believed to be patentable as well because they all are ultimately dependent on either claim 1, 7, or 12. Accordingly, the present invention distinguishes over Chen et al. for at least this reason. The Applicants respectfully submit that the Examiner's rejection under 35 U.S.C. § 102(e) has been overcome.

CONCLUSION

The remaining cited references have been reviewed and are not believed to affect the patentability of the claims as amended.

In this Response, Applicant has amended certain claims. In light of the Office Action, Applicant believes these amendments serve a useful clarification purpose, and are desirable for clarification purposes, independent of patentability. Accordingly, Applicants respectfully submit that the claim amendments do not limit the range of any permissible equivalents.

Applicant acknowledges the continuing duty of candor and good faith to disclosure of information known to be material to the examination of this application. In accordance with 37 CFR §1.56, all such information is dutifully made of record. The foreseeable equivalents of any territory surrendered by amendment are limited to the territory taught

---

[1] See MPEP §2131 (Emphasis Added) "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim."

by the information of record. No other territory afforded by the doctrine of equivalents is knowingly surrendered and everything else is unforeseeable at the time of this amendment by the Applicants and their attorneys.

Applicants respectfully submit that all of the grounds for rejection stated in the Examiner's Office Action have been overcome, and that all claims in the application are allowable. No new matter has been added. It is believed that the application is now in condition for allowance, which allowance is respectfully requested.

PLEASE CALL the undersigned if that would expedite the prosecution of this application.

Respectfully submitted,

Date: March 23, 2006

By: _____
Jeff Giunta, Reg. No. 42,583
Attorney for Applicants

FLEIT, KAIN, GIBBONS, GUTMAN BONGINI & BIANCO P.L.
551 N.W. 77th Street, Suite 111
Boca Raton, FL 33487
Tel (561) 989-9811
Fax (561) 989-9812